



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,607	07/12/2001	Yeong-Kwan Kim	249/258	1299

27849 7590 05/21/2003

LEE & STERBA, P.C.  
1101 WILSON BOULEVARD  
SUITE 2000  
ARLINGTON, VA 22209

EXAMINER

THOMAS, TONIAE M

ART UNIT	PAPER NUMBER
----------	--------------

2822

DATE MAILED: 05/21/2003

10

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/902,607

Applicant(s)

KIM ET AL.

Examiner

Toniae M. Thomas

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 07 February 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) 1-15 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 32-35 is/are allowed.
- 6) ☒ Claim(s) 16-20 is/are rejected.
- 7) ☒ Claim(s) 21-31 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 July 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. This action is an official response to the amendment filed on 07 February 2003. Currently, claims 1-35 are pending. Claims 1-15 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected invention, there being no allowable generic or linking claim.

#### ***Allowability Withdrawn***

2. The indicated allowability of claim 20 is withdrawn in view of the newly discovered reference(s) to Park et al. (US 6,326,282 B1). Rejections based on the newly cited reference follow.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. *Claims 16, 17, and 20 are rejected under 35 U.S.C. 103(a) as being obvious over Tu et al. (US 6,177,307 B1) in view of Park et al. (US 6,326,282 B1) and Gadgil et al. (US 5,879,459 B1).*<sup>1</sup>

The applied reference Park et al. (US 6,326,282 B1) has a common assignee and at least one common inventor with the instant application. Based upon the earlier

effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(I)(1) and § 706.02(I)(2).

Tu et al. disclose a method for fabricating a semiconductor device (see figs. 1A-1H and accompanying text). The method comprises: forming a trench 202, 204, 206, 208 in a semiconductor substrate 200 (fig. 1A), and forming a buried insulating layer filled in the trench without a void (fig. 1A and col. 2, lines 11-14).

Tu et al. do not teach the following limitations: forming a liner layer formed of a multi-layer of silicon nitride and silicon oxide on the sidewalls and bottom of the trench

---

<sup>1</sup> The Tu et al. patent was relied upon in the previous action.

by atomic layer deposition (ALD), wherein the liner layer is formed without breaking vacuum; and forming an oxide layer by thermal oxidation or ALD on the sidewalls and bottom of the trench before the liner layer is formed on the sidewalls and bottom of the trench.

Park et al. disclose a method for fabricating a semiconductor device that is compatible with Tu et al (figs. 2A-2E and accompanying). The method comprises: forming a trench 110 in a semiconductor substrate 100 (fig. 2B); forming a liner layer formed of a multi-layer of silicon nitride 114 and silicon oxide 115 on the sidewalls and bottom of the trench (fig. 2D and col. 4, lines 32-52); and forming a thermal oxide layer 112 on the sidewalls and bottom of the trench before the liner layer is formed on the sidewalls and bottom of the trench (fig. 2C and col. 4, lines 25-31). The oxide layer 115 is formed to protect the nitride layer 114, which serves as a stress relief layer and an oxidation barrier layer (col. 3, lines 35-38). The thermal oxide layer is formed prior to forming the liner layer so as to remove the damage caused by etching the substrate to form the trench.

The Gadgil et al. reference is relied upon in this action because it teaches that ALD is a better thin film coating method than the conventional CVD methods (col. 1, lines 34-37; col. 2, lines 42-49; col. 3, lines 38-60). One advantage of using ALD is: it provides uniformity and excellent step coverage (col. 1, lines 34-37). ALD has the ability to maintain ultra-uniform thin deposition layers over complex topology (col. 2, lines 42-49).

Gadgil et al. also teach that forming thin film layers without breaking vacuum is an inherent property of the ALD coating method (fig. 1a and col. 3, lines 5-20).

Since Tu et al., Park et al., and Gadgil et al. are from the same field of endeavor, the purpose disclosed by Park et al. and Gadgil et al. would have been recognized in the pertinent art of Tu et al.

One having ordinary skill in the art would have been motivated to modify Tu et al., at the time the invention was made, by forming a multi-layer of silicon nitride and silicon oxide on the sidewalls and bottom of the trench using atomic layer deposition, and forming a thermal oxide layer on the sidewalls and bottom of the trench prior to forming the silicon nitride/silicon oxide multi-layer because of the following reasons: the oxide layer protects the nitride layer, which serves as a stress relief layer and an oxidation barrier layer; the thermal oxide layer removes the damage to the substrate caused by etching the substrate to form the trench; and ALD provides a silicon nitride/silicon oxide multi-layer having uniformity and excellent step coverage.

4. *Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tu et al., Park et al., and Gadgil et al. as applied to claim 16 above, and further in view of Wolf et al. (Silicon Processing for the VLSI Era: Vol. 1 – Process Technology).*

Park et al. do not teach that the nitride layer is formed using a silicon source of silane, Si-alkoxide, Si-alkyl, Si-halide, or Si amide, and a nitrifying agent of ammonia, plasma ammonia, or plasma nitrogen; or that the silicon oxide layer is formed using a silicon source of silane, Si-alkoxide, Si-alkyl, Si-halide, or Si amide, and an oxidizing agent of water, hydrogen peroxide, ozone, plasma O<sub>2</sub>, N<sub>2</sub>O, or plasma N<sub>2</sub>O.

Wolf et al. disclose methods for forming silicon nitride and silicon oxide films. Wolf et al. teach forming silicon oxide films using silane as a silicon source and an oxidizing agent of  $N_2O$  (page 184, 4<sup>th</sup> par.), and forming silicon nitride films using silane as a silicon source and ammonia as the nitrifying agent (page 194, 1<sup>st</sup> par.).

One of ordinary skill in the art would have been motivated to modify the combination of Tu et al., Park et al., and Gadgil et al., at the time the invention was made, by forming the silicon oxide layer using silane and  $N_2O$  and forming the silicon nitride layer using silane and ammonia, as taught by Wolf et al., because: [1] a silicon oxide film that is formed by reacting silane and  $N_2O$  is less dense and has a high etch rate, and a silicon oxide film that is formed by reacting silane and ammonia has good step coverage.

### ***Allowable Subject Matter***

Claims 32-35 are allowable. The claims are allowable because the prior art of record does not anticipate, teach or suggest the following limitations recited in claim 32: [1] forming a first bubble prevention layer of a multi-layer of silicon oxide and silicon nitride on the gate spacers and the gate stack patterns by ALD, or [2] forming a second bubble prevention layer of a multi-layer of silicon oxide and silicon nitride on the bit line spacers and the bit line stack patterns by ALD.

6. Claims 21-31 are objected to as being dependent upon a rejected base claim, claim 16, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 21-31 would be

Art Unit: 2822

allowable if rewritten as discussed above for the following reason: the prior art of record does not anticipate, teach or suggest forming a first bubble prevention layer of a multi-layer of silicon oxide and silicon nitride on the gate spacers and the gate stack patterns by ALD, as recited in claim 21.

### **Conclusion**

5. Since the new ground of rejection presented in this Office action was not necessitated by amendment, this action is a non-final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (703) 305-7646. The examiner can normally be reached on Monday through Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

*TMT*

May 15, 2003

  
AMIR ZARABIAN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800